REMARKS

This paper is responsive to a final Office action dated January 23, 2006. Claims 1-25 were examined. Claims 1-7, 11, 15-17, and 24 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,118,316 to Tamamura et al. in view of U.S. Patent No. 6,353,648 B1 to Suzuki. Claims 10, 12, 13, 18, 19, 22, 23, and 25 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Tamamura in view of Suzuki and U.S. Patent No. 6,711,227 B1 to Kaylani et al. Claim 14 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Tamamura in view of Suzuki and U.S. Patent No. 5,036,298 to Bulzachelli. Claims 8, 9, 20, and 21 stand objected to as being dependent upon a rejected base claim.

Claim Rejections – 35 U.S.C. §103

Claims 1-7, 11, 15-17 and 24 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,118,316 to Tamamura et al. ("Tamamura") in view of U.S. Patent No. 6,353,648 B1 to Suzuki ("Suzuki").

Regarding claim 1, Applicants respectfully maintain that Tamamura, alone or in combination with Suzuki or other references of record, fails to teach or suggest

> a phase detector circuit coupled to generate a difference signal indicating a phase difference between an incoming data stream and a delayed clock signal; and a clock delay circuit coupled to receive a delay control signal derived from the difference signal and to receive the output clock signal, the clock delay circuit coupled to provide as the delayed clock signal the output clock signal delayed according to the delay control signal,

as required by claim 1. Tamamura teaches PLL 20A that divides an oscillation output signal 203a-1 by a division ratio in divider 204-1. Col. 8, lines 64-66; Fig. 4. Tamamura teaches that a divided signal 204a-1 is compared with input data 11-1 according to frequency and phase. Col. 8, line 66-col. 9, line 1; Fig. 4. The Office Action admits that Tamamura fails to teach or suggest

a clock delay circuit receiving a delay control signal derived from the difference signal and to receive an output clock signal, the clock delay circuit coupled to provide as a delayed clock signal the output clock signal delayed according to the delay control signal. The Office Action relies on delay device 7 of Suzuki to supply this teaching.

Suzuki teaches that delay device 7 has a delay time that varies according to a control signal corresponding to a phase comparison result. Col. 7, lines 12-17. The output of delay device 7 (i.e., timing signal 106) of Suzuki adjusts a logic decision period of internal circuit 6 by changing the delay of delay device 7 based on changes to the frequency of internal clock signal 105. Col. 5, lines 7-16; col. 6, lines 41-53. Suzuki teaches that the adjusted logic decision period of ensures proper operation of a dynamic circuit included in internal circuit 6 by preventing the output of internal circuit 6 from changing during a logic decision period. Col. 5, lines 7-16; col. 6, lines 41-53. Suzuki fails to teach or suggest that delay circuit 7 is in the feedback path of PLL 2 of Suzuki and fails to suggest the desirability of such modification to PLL 2 of Suzuki or to PLL 20A of Tamamura.

The Office action states that although Suzuki teaches that delay device 7 provides its output to an internal circuit 6, the output of the clock delay circuit may be provided to the phase comparator as taught by Tamamura to provide a more controlled delayed signal to the phase comparator of Tamamura. However, the Office action fails to provide a reference teaching the desirability of such modification to Suzuki or Tamamura. Rather, the Office engages in an impermissible hindsight analysis. See MPEP § 2142.

Thus, Applicants respectfully maintain that neither Tamamura, alone or in combination with Suzuki or other references of record, teaches or suggests a delayed clock signal being provided to a phase detector circuit based on a delay control signal derived from the difference signal generated by the phase detector circuit as required by claim 1. For at least this reason, Applicants believe that claim 1 is allowable over the art of record. Accordingly, Applicants respectfully request that the rejection of claim 1 and all claims dependent thereon, be withdrawn.

Regarding claim 15, Applicants respectfully maintain that Tamamura, alone or in combination with Suzuki or other references of record, fails to teach or suggest

> determining a phase difference between an input data stream and a delayed clock signal and generating a difference signal indicative thereof; and receiving the output clock signal in a delay circuit and generating the delayed clock signal from the output clock signal according to a delay control signal derived from the difference signal,

as required by claim 15. Tamamura teaches PLL 20A that divides an oscillation output signal 203a-1 by a division ratio in divider 204-1. Col. 8, lines 64-66; Fig. 4. Tamamura teaches that a divided signal 204a-1 is compared with input data 11-1 according to frequency and phase. Col. 8, line 66-col. 9, line 1; Fig. 4. The Office Action admits that Tamamura fails to teach or suggest a clock delay circuit receiving a delay control signal derived from the difference signal and to receive an output clock signal, the clock delay circuit coupled to provide as a delayed clock signal the output clock signal delayed according to the delay control signal. The Office Action relies on delay device 7 of Suzuki to supply this teaching.

Suzuki teaches that delay device 7 has a delay time that varies according to a control signal corresponding to a phase comparison result. Col. 7, lines 12-17. The output of delay device 7 (i.e., timing signal 106) of Suzuki adjusts a logic decision period of internal circuit 6 by changing the delay of delay device 7 based on changes to the frequency of internal clock signal 105. Col. 5, lines 7-16; col. 6, lines 41-53. Suzuki teaches that the adjusted logic decision period of ensures proper operation of a dynamic circuit included in internal circuit 6 by preventing the output of internal circuit 6 from changing during a logic decision period. Col. 5, lines 7-16; col. 6, lines 41-53. Suzuki fails to teach or suggest that delay circuit 7 is in the feedback path of PLL 2 of Suzuki and fails to suggest the desirability of such modification to PLL 2 of Suzuki or to PLL 20A of Tamamura.

The Office action states that although Suzuki teaches that delay device 7 provides its output to an internal circuit 6, the output of the clock delay circuit may be provided to the phase comparator as taught by Tamamura to provide a more controlled delayed signal to the phase comparator of Tamamura. However, the Office action fails to provide a reference teaching the

desirability of such modification to Suzuki or Tamamura. Rather, the Office engages in an impermissible hindsight analysis. See MPEP § 2142.

Thus, Applicants respectfully maintain that neither Tamamura, alone or in combination with Suzuki or other references of record, teaches or suggests determining a phase difference between an input data stream and a delayed clock signal and generating a difference signal indicative thereof and receiving the output clock signal in a delay circuit and generating the delayed clock signal from the output clock signal according to a delay control signal derived from the difference signal, as required by claim 15. For at least this reason, Applicants believe that claim 15 is allowable over the art of record. Accordingly, Applicants respectfully request that the rejection of claim 15 and all claims dependent thereon, be withdrawn.

Regarding claim 24, Applicants respectfully maintain that Tamamura, alone or in combination with Suzuki or other references of record fails to teach or suggest

> means for detecting a phase difference between an incoming data stream and a delayed clock signal and generating a difference signal indicative thereof; and means for generating the delayed clock signal from the clock signal according to a delay control signal derived from the difference signal,

as required by claim 24. Tamamura teaches PLL 20A that divides an oscillation output signal 203a-1 by a division ratio in divider 204-1. Col. 8, lines 64-66; Fig. 4. Tamamura teaches that a divided signal 204a-1 is compared with input data 11-1 according to frequency and phase. Col. 8, line 66-col. 9, line 1; Fig. 4. The Office Action admits that Tamamura fails to teach or suggest a clock delay circuit receiving a delay control signal derived from the difference signal and to receive an output clock signal, the clock delay circuit coupled to provide as a delayed clock signal the output clock signal delayed according to the delay control signal. The Office Action relies on delay device 7 of Suzuki to supply this teaching.

Suzuki teaches that delay device 7 has a delay time that varies according to a control signal corresponding to a phase comparison result. Col. 7, lines 12-17. The output of delay

device 7 (i.e., timing signal 106) of Suzuki adjusts a logic decision period of internal circuit 6 by changing the delay of delay device 7 based on changes to the frequency of internal clock signal 105. Col. 5, lines 7-16; col. 6, lines 41-53. Suzuki teaches that the adjusted logic decision period of ensures proper operation of a dynamic circuit included in internal circuit 6 by preventing the output of internal circuit 6 from changing during a logic decision period. Col. 5, lines 7-16; col. 6, lines 41-53. Suzuki fails to teach or suggest that delay circuit 7 is in the feedback path of PLL 2 of Suzuki and fails to suggest the desirability of such modification to PLL 2 of Suzuki or to PLL 20A of Tamamura.

The Office action states that although Suzuki teaches that delay device 7 provides its output to an internal circuit 6, the output of the clock delay circuit may be provided to the phase comparator as taught by Tamamura to provide a more controlled delayed signal to the phase comparator of Tamamura. However, the Office action fails to provide a reference teaching the desirability of such modification to Suzuki or Tamamura. Rather, the Office engages in an impermissible hindsight analysis. See MPEP § 2142.

Thus, Applicants respectfully maintain that neither Tamamura, alone or in combination with Suzuki or other references of record, teaches or suggests means for detecting a phase difference between an incoming data stream and a delayed clock signal and generating a difference signal indicative thereof and means for generating the delayed clock signal from the clock signal according to a delay control signal derived from the difference signal, as required by claim 24. For at least this reason, Applicants believe that claim 24 is allowable over the art of record. Accordingly, Applicants respectfully request that the rejection of claim 24 and all claims dependent thereon, be withdrawn.

Claims 10, 12, 13, 18, 19, 22, 23 and 25 are rejected under 35 U.S.C. §103(a) as being unpatentable over Tamamura in view of Suzuki and U.S. Patent No. 6,711,227 B1 to Kaylani et al. Applicants respectfully maintain that claims 10, 12, 13, 18, 19, 22, 23, and 25 depend from allowable base claims and are allowable for at least this reason. Accordingly, Applicants respectfully request that the rejection of these claims be withdrawn.

Claim 14 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Tamamura, et al. in view of Suzuki and U.S. Patent 5,036,298 to Bulzachelli. Applicants respectfully

maintain that claim 14 depends from an allowable base claim and is allowable for at least this reason. Accordingly, Applicants respectfully request that the rejection of claim 14 be withdrawn.

Allowable Subject Matter

Applicants appreciate the indication of allowable subject matter in claims 8, 9, 20, and 21. Claim 8 is amended to include limitations of claim 1, claim 6, and claim 7, from which claim 8 depends, thus putting claims 8 and 9 in condition for allowance.

Claim 20 is amended to correct a typographical error. Applicants respectfully maintain that claims 20 and 21 depend from allowable base claims and are allowable for at least this reason. Accordingly, Applicants respectfully request that the objections to these claims be withdrawn.

In summary, claims 1-25 are in the case. All claims are believed to be allowable over the art of record, and a Notice of Allowance to that effect is respectfully solicited. Nonetheless, if any issues remain that could be more efficiently handled by telephone, the Examiner is requested to call the undersigned at the number listed below.

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